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EXAMINER	
HENDERSON, ADAM	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/684,706	DONG, KIMBLE	
	Examiner	Art Unit	
	Adam L. Henderson	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

14

1)☒ Responsive to communication(s) filed on May 2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3, 5, 7-9, 12-15, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (US Patent 6,611,288) in view of Ackland et al. ('Camera on a Chip').

4. With regard to claim 1 Fossum et al. disclose a MOS image sensor comprising:

a pixel array formed from a plurality of pixels arranged in a matrix of rows and columns (FIG. 2, column 3 lines 1-23);

location processing means for providing a digital location number for each pixel of the pixel array (column 2 line 63 – column 3 line 65) [the system stores and compares the location addresses, therefore there must inherently be some means for providing the location addresses of the individual pixels];

signal processing circuitry for reading out signals from the pixel array and outputting processed pixel signals (column 2 line 15 – column 3 line 65);

dead pixel comparator circuitry for receiving the processed pixel signals from the signal processing circuitry and examining the processed pixel signals to see if they are indicative of dead pixels (column 2 lines 15-65);

location storage circuitry for receiving dead pixel information from the dead pixel comparator circuitry and for storing the digital location number generated by the location processing means for each dead pixel(register 300, column 2 lines 63-65); and

location comparator circuitry for comparing the digital location number of a pixel that is being processed by the signal processing circuitry with the stored digital location numbers of dead pixels to determine if the pixel that is being processed corresponds to a dead pixel (column 3 lines 55-65), but fails to disclose wherein the pixel array and the dead pixel comparator circuitry is formed on a single integrated circuit.

Ackland et al. disclose a MOS pixel array and signal control/processing formed on a single integrated circuit (page 24, column 1, first full paragraph).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor taught by Fossum et al. to include the single chip features taught by Ackland et al. in order to improve noise (Ackland et al. page 24, column 1, paragraphs 1-3).

5. With regard to claim 3 Fossum et al. disclose the image sensor of claim 1, wherein the signal processing circuitry compensates for a dead pixel by repeating a pixel signal from a pixel that was read out prior to the dead pixel (column 3 line 66 – column 4 line 7).

6. With regard to claim 5 Fossum et al. disclose the image sensor of claim 1, wherein the dead pixel comparator is initially activated when the image sensor is first powered on to examine the processed pixel signals from each pixel only once (column 2 lines 20-22).

7. With regard to claim 7 Fossum et al. disclose The image sensor of claim 1, wherein the location storage circuitry is coupled to an off chip storage area (register 300, column 2 lines 63-65).

8. With regard to claim 8 Fossum et al. disclose a method for correcting for dead pixels in a MOS imaging array, said imaging array including a plurality of pixels arranged in a matrix of rows and columns, said method comprising the steps of:

sequentially examining the signals from each pixel in the imaging array to determine if each pixel is a dead pixel (column 2 line 15 – column 3 line 23);

storing a location number of each dead pixel into a reprogrammable memory (column 2 lines 63-65);

after all of the dead pixels have been determined and their location numbers stored, proceeding with normal image processing of the imaging array, during which as the signal from each pixel is read out, the location number of each pixel is compared with the stored location numbers for dead pixels, and the signal from any pixel with a location number that corresponds to the stored location number of a dead pixel is compensated for (column 3 line 24 – column 4 line 27).

Fossum et al. fail to disclose the image sensor is of MOS type.

Ackland et al. disclose a MOS pixel array and signal control/processing formed on a single integrated circuit (page 24, column 1, first full paragraph).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor taught by Fossum et al. to include the single chip features taught by Ackland et al. in order to improve noise (Ackland et al. page 24, column 1, paragraphs 1-3).

9. Claim 9 is rejected under the same analysis as claim 3.

10. With regard to claim 12 Fossum et al. disclose the method of claim 8, wherein a location comparator is used to perform the step of comparing the location number of a pixel with a stored location number for a dead pixel (column 3 lines 55-65).

11. With regard to claim 13 Fossum et al. disclose the method of claim 8, wherein the stored location numbers of the dead pixels may be updated by repeating the steps of sequentially examining the signals from each pixel in the imaging array to determine if each pixel is a dead pixel and then storing the location numbers of each dead pixel (column 2 lines 20-22) [the locations are updated with each start-up].

12. With regard to claim 14 Fossum et al. disclose a method for correcting for dead pixels in a MOS imaging array, said imaging array including a plurality of pixels arranged in a matrix of rows and columns, said method comprising the steps of:

(a) reading out a pixel signal from a pixel in the pixel array (column 2 line 15 – column 3 line 23);

(b) determining if the pixel signal from the pixel indicates that the pixel is a dead pixel (column 2 line 15 – column 3 line 23);

(c) storing a location number of a dead pixel (column 2 lines 63-65);

(d) repeating steps (a) to (c) for each pixel in the pixel array until all of the pixels have been read out (column 2 line 15 – column 3 line 23);

(e) thereafter comparing the location number of each pixel that is being read out with the stored location numbers of dead pixels and compensating for the signal from a pixel whose

location number corresponds to the stored location number of a dead pixel (column 3 line 24 – column 4 line 27); and

(f) repeating steps (a) to (e) each time the imaging array is powered on for normal operation (column 2 lines 20-22).

Fossum et al. fail to disclose the image sensor is of MOS type.

Ackland et al. disclose a MOS pixel array and signal control/processing formed on a single integrated circuit (page 24, column 1, first full paragraph).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor taught by Fossum et al. to include the single chip features taught by Ackland et al. in order to improve noise (Ackland et al. page 24, column 1, paragraphs 1-3).

13. Claim 15 is rejected under the same analysis as claim 3.

14. With regard to claim 17 Fossum et al. disclose the method of claim 14, wherein the stored location numbers of the dead pixels may be updated by repeating steps (a) to (d) (column 2 lines 20-22).

15. With regard to claim 18 Fossum et al. disclose a method for correcting for dead pixels in a MOS imaging array, said imaging array including a plurality of pixels arranged in a matrix of rows and columns, said method comprising the steps of:

(a) generating a location number for a pixel in the imaging array and reading out the signal from the pixel (column 2 line 15 – column 3 line 23);

(b) determining if the signal from the pixel indicates that the pixel is a dead pixel (column 2 line 15 – column 3 line 23);

(c) updating data stored in a storage area stored during a previous initialization of the MOS imaging array, wherein said updating data includes storing the location number of the dead pixel in the storage area if the signal from the pixel indicates that the pixel is a dead pixel, storing the location number of the dead pixel in a storage area (column 2 lines 20-65);

(d) repeating steps (a) to (c) until all of the pixels have been read out (column 2 line 15 – column 3 line 23);

(e) after all of the pixels have initially been read out and the dead pixel location numbers have been stored, reading out a signal from a pixel in the pixel array (column 3 line 24 – column 4 line 27);

(f) comparing the location number of the pixel that is currently being read with the stored location numbers of the dead pixels (column 3 line 24 – column 4 line 27);

(g) compensating for a pixel whose location number corresponds to a stored location number of a dead pixel (column 3 line 24 – column 4 line 27); and

(h) repeating steps (e) to (g) for all of the pixels in the pixel array to produce each frame of the image signal (column 3 line 24 – column 4 line 27).

Fossum et al. fail to disclose the image sensor is of MOS type.

Ackland et al. disclose a MOS pixel array and signal control/processing formed on a single integrated circuit (page 24, column 1, first full paragraph).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor taught by Fossum et al. to include the single chip features taught by Ackland et al. in order to improve noise (Ackland et al. page 24, column 1, paragraphs 1-3).

16. Claim 19 is rejected under the same analysis as claim 3.

17. Claims 2, 11, and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (US Patent 6,611,288) in view of Ackland et al. ('Camera on a Chip') as applied to claims 1, 8, 14, and 18 above, and further in view of Younse et al. (US Patent 4,805,023).

18. With regard to claim 2 Fossum et al. and Ackland et al. disclose the image sensor of claim 1, but fail to disclose wherein the location processing means comprises a location shift register for indicating the digital location number of each of the pixels to the pixel array, the location comparator circuitry, and the location storage circuitry.

Younse et al. disclose wherein the location processing means comprises a location shift register for indicating the digital location number of each of the pixels to the pixel array, the location comparator circuitry, and the location storage circuitry (pixel address counter, column 3 lines 1-30).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor of Fossum et al. and Ackland et al. to include the pixel address counter of Younse et al. in order to know the exact pixel address currently being scanned (Younse et al, column 3 lines 1-30).

19. Claim 11 is rejected under the same analysis as claim 2.

20. With regard to claim 21 Fossum et al. disclose an image sensor comprising:

a pixel array formed from a plurality of pixels arranged in a matrix of rows and columns (FIG. 2, column 3 lines 1-23);

signal processing circuitry for reading out signals from the pixel array and outputting processed pixel signals (column 3 line 24 – column 4 line 27);

dead pixel comparator circuitry for receiving the processed pixel signals from the signal processing circuitry and examining the processed pixel signals to see if they are indicative of dead pixels (column 2 lines 20-65), and for indicating when the location number of a pixel that is determined to be a dead pixel should be stored (column 2 lines 63-65),

Fossum et al. fails to disclose a location shift register for incrementing location numbers for pixels in the pixel array; and wherein the pixel array and the dead pixel comparator circuitry are formed on a single integrated circuit.

Younse et al. disclose wherein the location processing means comprises a location shift register for indicating the digital location number of each of the pixels to the pixel array, the location comparator circuitry, and the location storage circuitry (pixel address counter, column 3 lines 1-30).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor of Fossum et al. and Ackland et al. to include the pixel address counter of Younse et al. in order to know the exact pixel address currently being scanned (Younse et al, column 3 lines 1-30).

Ackland et al. disclose a MOS pixel array and signal control/processing formed on a single integrated circuit (page 24, column 1, first full paragraph).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor taught by Fossum et al. to include the single chip features taught by Ackland et al. in order to improve noise (Ackland et al. page 24, column 1, paragraphs 1-3).

21. With regard to claim 22 Ackland discloses the image sensor of claim 21, wherein the pixel array, the signal processing circuitry, the location shift register and the dead pixel comparator circuitry are fabricated on a single MOS chip (page 24, column 1, paragraphs 1-3).

22. With regard to claim 23 Fossum et al. disclose the image sensor of claim 21, further comprising location storage circuitry for storing the location numbers of dead pixels (registers 300, column 2 lines 63-65).

23. With regard to claim 24 Fossum et al. disclose the image sensor of claim 23, further comprising location comparator circuitry for comparing the location number of a pixel that is being processed by the signal processing circuitry with the stored location numbers of dead pixels from the location storage circuitry to determine if the pixel that is being processed corresponds to a dead pixel (column 3 line 24 – column 4 line 27).

24. Claims 4, 10, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (US Patent 6,611,288) in view of Ackland et al. ('Camera on a Chip') as applied to claims 1, 8, 14, and 18 above, and further in view of Lin et al. (US Patent 4,920,428).

25. With regard to claim 4 Fossum et al. and Ackland et al. disclose the image sensor of claim 1, but fail to disclose wherein the signal processing circuitry compensates for a dead pixel by averaging the pixel signal from a pixel that was read out prior to the dead pixel with a pixel signal from a pixel that is read out subsequent to the dead pixel.

Lin et al. disclose wherein the signal processing circuitry compensates for a dead pixel by averaging the pixel signal from a pixel that was read out prior to the dead pixel with a pixel signal from a pixel that is read out subsequent to the dead pixel (column 6 lines 1-2).

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor of Fossum et al. and Ackland et al. to include the pixel averaging function taught by Lin et al. in order to provide an alternative method that is well known. Fossum et al. admits the substitution method could be more complicated than he describes, for instance Fossum discloses a median function is another possibility (Fossum et al, column 4 lines 20-22). Therefore it would be obvious that the mean pixel value taught by Lin would be equally valid method of pixel replacement.

26. Claims 10, 16, and 20 are rejected under the same analysis as claim 4.

27. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (US Patent 6,611,288) in view of Ackland et al. ('Camera on a Chip') as applied to claim 5 above, and further in view of Katoh et al. (US Patent 5,796,430).

28. With regard to claim 6 Fossum et al. and Ackland et al. disclose the MOS image sensor of claim 5. but fail to disclose wherein the dead pixel comparator may be activated at later times to reexamine the processed pixel signals from each pixel so as to update the dead pixel digital location numbers stored in the location storage circuitry.

Katoh et al. disclose wherein the dead pixel comparator may be activated at later times to reexamine the processed pixel signals from each pixel so as to update the dead pixel digital location numbers stored in the location storage circuitry (column 6 lines 23-41) [turning the system off may also activate the detection process].

It would have been obvious at the time of the invention to one of ordinary skill in the art to modify the image sensor of Fossum et al. and Ackland et al. to include the update feature

taught by Katoh et al. in order to provide a further check to ensure that all dead pixels were detected by the camera.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam L. Henderson whose telephone number is 571-272-8619. The examiner can normally be reached on Monday-Friday, 7am to 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ALH
5 September 2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER